A Customizable Simulation Model of an ATM/SONET Framer for System Level Verification and Performance Characterization

ABSTRACT

This system represents a customizable simulation model of an ATM/SONET Framer for System Level Verification and Performance Characterization.An Asynchronous Transfer Mode (ATM) data processing ASIC interfaces with a Media Access Control (MAC) device that presents an electrical data path interface, called Universal Test & Operations PHY Interface for ATM (UTOPIA), using ATM protocol on the ASIC side and simplex optical interfaces using Synchronous Optical Network (SONET) protocol on the network side. Such a MAC device, commonly referred to as ATM/SONET Framer, provides one Receive and one Transmit interface to the network at various SONET line rates such as 155.52 Mbps(OC-3), 622.08 Mbps(OC-12), 2488.32 Mbps(OC-48), etc. The ATM and the SONET interfaces operate on different clock frequencies and thus represent two distinct clocking domains. The data interchange between the two clocking domains is achieved via FIFO buffer elements and associated control and status signals.